

SEMICONDUCTOR DEVICE, SEMICONDUCTOR DEVICE PACKAGE, AND LIGHTNING APPARATUS

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application is a divisional of U.S. application Ser. No. 14/729,619, filed on Jun. 3, 2015, which claims the benefit of priority from Korean Patent Application No. 10-2014-0154974 filed on Nov. 10, 2014, with the Korean Intellectual Property Office, the entire contents of each of which are hereby incorporated by reference herein.

BACKGROUND

[0002] Example embodiments relate to a semiconductor device, a semiconductor device package, and/or a lighting apparatus.

[0003] A solder bump formed on an electrode or a semiconductor chip including a light emitting diode (LED) may be formed by forming a solder on an under bump metallurgy (UBM) layer and reflowing the solder.

[0004] Due to a phase change in the solder during the reflow process, an intermetallic compound (IMC) formed between the solder and the UBM layer may diffuse into lateral surfaces of the UBM layer due to wettability of the UBM layer, so as to be in contact with the electrode. Residual stress generated by the phase change may cause cracks in the IMC in a relatively brittle portion thereof, in contact with the electrode, whereby the solder bump may be separated from the electrode.

SUMMARY

[0005] Example embodiments may provide a plan of reducing or substantially preventing an occurrence of cracks in an intermetallic compound (IMC).

[0006] According to example embodiments, a semiconductor device may include a light emitting structure and second conductivity-type semiconductor layers formed of or including $\text{Al}_x\text{In}_y\text{Ga}_{(1-x-y)}\text{N}$, wherein $0 \leq x < 1$, $0 \leq y < 1$, and $0 \leq x+y < 1$, and an active layer disposed between the first and second conductivity-type semiconductor layers, and an interconnection bump including an under bump metallurgy (UBM) layer disposed on an electrode of at least one of the first and second conductivity-type semiconductor layers, and having a first surface disposed opposite to a surface of the electrode and a second surface extending from an edge of the first surface to be connected to the electrode, an intermetallic compound (IMC) disposed on the first surface of the UBM layer, a solder bump bonded to the UBM layer with the IMC therebetween, and a barrier layer disposed on the second surface of the UBM layer and substantially preventing the solder bump from being diffused into the second surface of the UBM layer.

[0007] A formation of the IMC or the solder bump may be absent from the barrier layer.

[0008] The barrier layer may include an oxide layer containing at least one element of the UBM layer.

[0009] The barrier layer may include an oxide layer containing at least one of nickel (Ni) and copper (Cu).

[0010] The barrier layer may have a lower level of wettability with respect to the IMC and the solder bump than a level of wettability with respect to the UBM layer.

[0011] The second surface of the UBM layer may have a structure slightly inclined towards the electrode from the first surface of the UBM layer.

[0012] The second surface of the UBM layer may be substantially perpendicular to the surface of the electrode.

[0013] The UBM layer may have a multilayer structure including a titanium (Ti) layer in contact with the electrode, and a Ni layer or a Cu layer disposed on the Ti layer.

[0014] The UBM layer may have a multilayer structure including a chromium (Cr) layer in contact with the electrode, and a Ni layer or a Cu layer disposed on the Cr layer.

[0015] The UBM layer may have a monolayer structure formed as or including one of a Ni layer or a Cu layer.

[0016] The semiconductor device may further include a passivation layer disposed adjacently to the UBM layer on the electrode.

[0017] The passivation layer may be disposed to be separated from the UBM layer by being spaced apart therefrom, on the electrode.

[0018] The passivation layer may have a thickness that is lower than a thickness of the UBM layer.

[0019] According to example embodiments, a semiconductor device may include a light emitting structure including a plurality of electrodes and an interconnection bump disposed on the plurality of electrodes, wherein the interconnection bump includes a UBM layer disposed on the electrode, the UBM layer having a first surface disposed opposite to a surface of the electrode and a second surface extending from an edge of the first surface to be connected to the electrode, an IMC disposed on the first surface of the UBM layer, a solder bump bonded to the UBM layer with the IMC therebetween, and a barrier layer disposed on the second surface of the UBM layer, the barrier layer substantially preventing the solder bump from being diffused into the second surface of the UBM layer.

[0020] The plurality of electrodes may be disposed in a single direction in the light emitting structure.

[0021] The light emitting structure may include first and second conductivity-type semiconductor layers formed of or including $\text{Al}_x\text{In}_y\text{Ga}_{(1-x-y)}\text{N}$, wherein $0 \leq x < 1$, $0 \leq y < 1$, and $0 \leq x+y < 1$, and an active layer disposed between the first and second conductivity-type semiconductor layers.

[0022] According to example embodiments, a semiconductor device package may include a package main body, a semiconductor device mounted on the package main body, and an encapsulating portion encapsulating the semiconductor device.

[0023] The encapsulating portion may contain at least one type of phosphor.

[0024] According to example embodiments, a lighting apparatus may include a housing, and at least one semiconductor device package in the housing.

[0025] The lighting apparatus may further include a cover unit installed in the housing and encapsulating the at least one semiconductor device package.

BRIEF DESCRIPTION OF DRAWINGS

[0026] The above and other features and advantages or example embodiments will be more clearly understood from the following detailed description taken in conjunction with the accompanying drawings, in which:

[0027] FIG. 1 is a cross-sectional view schematically illustrating an interconnection bump of a semiconductor device according to an example embodiment;